Digital Logic Fundamentals

The University of Toledo
Electrical Engineering Technology
EET 2210

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Office Hours: 1:00PM-2:00PM M, 8:00-12:00 T
Office Location: NE 1624
Instructor Phone: 419-530-3896

Offered: Fall 2018

Class Location: PL3050
Class Day/Time: Section 001: 8:00-9:20 – M, W
Lab Location: NE2380
Lab Day/Time: Section 002:9:25-11:05 – M
Section 003:9:25-11:05 – W
Website or Blackboard: Blackboard
Credit Hours: 4 (Lecture: 3hours, Lab:2 hours)

CATALOG/COURSE DESCRIPTION

This course covers the fundamentals of digital logic circuits. Topics include number systems, logic gates, Boolean algebra, logic simplification, Karnaugh maps, adders, multipliers, multiplexers and decoders. Elementary digital circuits including flip-flops, counters, shift registers, memory devices, programmable logic devices and integrated circuits are also covered.

COURSE OBJECTIVES

In this course students are expected to:
1. Develop an understanding of the analytical techniques used in digital logic.
2. Develop an understanding of the laboratory skills used to evaluate digital circuits.
3. Analyze and interpret laboratory data from basic digital logic circuits.
4. Work effectively in the laboratory with lab partners.
5. Identify and solve programs related to digital logic circuits.

ABET STUDENT LEARNING OUTCOMES

a. An understanding of the analytical and laboratory skills associated with electrical engineering technology.
b. An ability to apply current knowledge and adapt to emerging applications of mathematics, science and technology.
c. An ability to conduct, analyze, and interpret experiments concerning digital circuits.
d. An ability to use creativity in the design and use of digital systems and processes.
e. An ability to function as part of a team.
f. An ability to identify, analyze and solve technical problems associated with digital systems design.
g. An ability to communicate effectively.
k. A commitment to quality and continuous improvement.

PREREQUISITES

EET-1010 Resistive Circuits

REQUIRED INSTRUCTIONAL MATERIALS (available at the bookstore)

Digital Fundamentals Conventional Current Version, 11th Ed., Floyd, 2015
Experiments in Digital Fundamentals, Buchla & Joksch, 2013
Lab Kit

COURSE OUTLINE- MAJOR CONTENT AREAS

- Use of different number systems, operations, and codes
- Introduction to logic gates
- Familiarization with Boolean Algebra and logic simplification
- Familiarization with Combinational Logic
- Familiarization with functions of combinational logic
- Introduction to flip-flops and related devices
- Introduction to Counters
- Introduction to Counter Design
- Introduction to Shift Registers
- Introduction to memory types and storage
- Integrated circuit technologies

COURSE OUTLINE- MAJOR LABORATORY TOPICS

- Construction of a Logic Probe
- Number systems
- Logic Gates
- Interpreting Manufacturer's Data Sheets
- Boolean Laws and DeMorgan's Theorem
- Logic Circuit simplification
- Adder and Magnitude Comparator
- Combinational logic using multiplexers
- The D latch and D flip-flop
- The J-K flip-flop

UNIVERSITY POLICIES

Academic Accommodations

The University of Toledo is committed to providing equal opportunity and access to the educational experience through the provision of reasonable accommodations. For students who have an accommodations memo from Student Disability Services, it is essential that you correspond with me as soon as possible to discuss your disability-related accommodation needs for this course. For students not registered with Student Disability Services who would like information regarding eligibility for academic accommodations due to barriers associated with a potential disability, please contact the Student Disability Services Office.)

COURSE EXPECTATIONS

1. *All assignments including homework are graded based on correctness.*
2. *All assignments are to be completed on time and turned in at the beginning of the class/lab.*
3. *You will be responsible for all materials covered in class as well as the material assigned in the book.*

4. There are no make-up exams for this course. If you have a problem or conflict and cannot attend an exam, let me know beforehand and we will try to work something out. No credit will be given for a missed exam that we haven't made arrangements about beforehand unless you have a really excusable emergency. Cell phone use will not be allowed.

5. Cheating and Academic dishonesty is not allowed and will be punished by rules of University of Toledo Student Handbook. Read this http://www.utoledo.edu/policies/academic/undergraduate/pdfs/3364-71-04%20%20Academic%20dishonesty.pdf

OVERVIEW OF COURSE GRADE ASSIGNMENT

Homework 11%, Quizzes 11%, Lab 28%, Midterm Test 1 20%, Final Exam 30 % (Comprehensive)
A >= 90, B >= 80, C > = 70, D > = 60

COURSE GUIDELINES

Homework assignments are accepted only before or on the assigned day. Homework are graded on correctness. The final answer alone is not enough to get credit. Solution steps must be shown to get credit.

TENTATIVE COURSE SCHEDULE

Date	Week	Chapter	Test	Lab	Quiz on Wed.	Homework	Assigned on	Due on
27-Aug	1	Ch.1		NO LAB		ch1	29-Aug	10-Sep
3-Sep	2	NO CLASS		NO LAB				
10-Sep	3	Ch.2		Exp#2: Construction of a Logic Probe	ch1	ch2	10-Sep	17-Sep
17-Sep	4	Ch.3		Exp#3: Number systems	ch2	ch3	17-Sep	24-Sep
24-Sep	5	Ch.4		Exp#4: Logic Gates	ch3	ch4	24-Sep	1-Oct
1-Oct	6	Ch.5		Exp#6: Interpreting Manufacturer's Data Sheets	ch4	ch5	1-Oct	8-Oct
8-Oct	7	Review Ch 1-5	**Test1 Wed. Oct. 10 8AM-9.20AM**	NO LAB				
15-Oct	8	Ch.6		Exp#7: Boolean Laws and DeMorgan's Theorem		ch6	15-Oct	22-Oct
22-Oct	9	Ch.7		Exp#8: Logic Circuit simplification	ch6	ch7	22-Oct	29-Oct
29-Oct	10	Ch.8		Exp#11: Adder and Magnitude Comparator	ch7	ch8	29-Oct	5-Nov
5-Nov	11	Ch.9		Exp#12: Combinational logic using multiplexers	ch8	ch9	5-Nov	14-Nov
12-Nov	12	Ch.10		Exp#14: The D latch and D flip-flop (Veterans day)	ch9			
19-Nov	13	Ch.11		Exp#14: The D latch and D flip-flop (Thanksgiving)		ch 10 & 11	14-Nov	26-Nov
26-Nov	14	Ch.11 & 12		Exp#16: The J-K flip-flop	ch10 &11	ch12	26-Nov	3-Dec
3-Dec	15	12 + Review		Exp#16: The J-K flip-flop				
10-Dec	15		**Final Test Mon. Dec 10 8AM-10AM**					

Midterm Test on Wednesday October 10 8:00AM-9:20AM

Final Test on Monday December 10, 8:00AM-10:00AM

I have received and read the syllabus.

Printed Student Name……..

Signature……Date……..