Digital Logic Fundamentals

The University of Toledo
Electrical Engineering Technology
EET 2210

Name: Dr. Ngalula Sandrine Mubenga, PhD, PE
Email: ngalula.mubenga@utoledo.edu
Office Hours: 9:30AM-12:00PM - M, W
Office Location: NE 1624
Instructor Phone: 419-530-3896

Offered: Fall 2019

Class Location: PL3050
Class Day/Time: Section 001: 8:00-9:20 – M, W
Lab Location: NE2380/ NE2330
Lab Day/Time: Section 002:9:25-11:05 – M
Section 003:9:25-11:05 – W
Website or Blackboard: Blackboard
Credit Hours: 4

CATALOG/COURSE DESCRIPTION

This course covers the fundamentals of digital logic circuits. Topics include number systems, logic gates, Boolean algebra, logic simplification, Karnaugh maps, adders, multipliers, multiplexers and decoders. Elementary digital circuits including flip-flops, counters, shift registers, memory devices, programmable logic devices and integrated circuits are also covered.

COURSE OBJECTIVES

In this course students are expected to:
1. Develop an understanding of the analytical techniques used in digital logic.
2. Develop an understanding of the laboratory skills used to evaluate digital circuits.
3. Analyze and interpret laboratory data from basic digital logic circuits.
4. Work effectively in the laboratory with lab partners.
5. Identify and solve problems related to digital logic circuits.

ABET STUDENT LEARNING OUTCOMES

a. An understanding of the analytical and laboratory skills associated with electrical engineering technology.
b. An ability to apply current knowledge and adapt to emerging applications of mathematics, science and technology.
c. An ability to conduct, analyze, and interpret experiments concerning digital circuits.
d. An ability to use creativity in the design and use of digital systems and processes.
e. An ability to function as part of a team.
f. An ability to identify, analyze and solve technical problems associated with digital systems design.
g. An ability to communicate effectively.
k. A commitment to quality and continuous improvement.

PREREQUISITES

EET-1010 Resistive Circuits

REQUIRED INSTRUCTIONAL MATERIALS (available at the bookstore)
Digital Fundamentals Conventional Current Version, 11th Ed., Floyd, 2015
Experiments in Digital Fundamentals, Buchla & Joksch, 2013
Lab Kit

COURSE OUTLINE- MAJOR CONTENT AREAS
- Use of different number systems, operations, and codes
- Introduction to logic gates
- Familiarization with Boolean Algebra and logic simplification
- Familiarization with Combinational Logic
- Familiarization with functions of combinational logic
- Introduction to flip-flops and related devices
- Introduction to Counters
- Introduction to Counter Design
- Introduction to Shift Registers
- Introduction to memory types and storage
- Integrated circuit technologies

COURSE OUTLINE- MAJOR LABORATORY TOPICS
- Construction of a Logic Probe
- Number systems
- Logic Gates
- Interpreting Manufacturer's Data Sheets
- Boolean Laws and DeMorgan's Theorem
- Logic Circuit simplification
- Adder and Magnitude Comparator
- Combinational logic using multiplexers
- The D latch and D flip-flop
- The J-K flip-flop

UNIVERSITY POLICIES

Academic Accommodations

The University of Toledo is committed to providing equal opportunity and access to the educational experience through the provision of reasonable accommodations. For students who have an accommodations memo from Student Disability Services, it is essential that you correspond with me as soon as possible to discuss your disability-related accommodation needs for this course. For students not registered with Student Disability Services who would like information regarding eligibility for academic accommodations due to barriers associated with a potential disability, please contact the Student Disability Services Office.)

COURSE EXPECTATIONS
1. *All assignments including homework are graded based on correctness.*
2. *All assignments are to be completed on time and turned in at the beginning of the class/lab.*
3. *You are responsible for all materials covered in class as well as the material assigned in the book.*
4. *There is no make-up quiz, exams or homework for this course.*

5. *Cheating and Academic dishonesty is not allowed and will be punished by rules of University of Toledo Student Handbook. Read this* *http://www.utoledo.edu/policies/academic/undergraduate/pdfs/3364-7104%20%20Academic%20dishonesty.pdf*

Electronica Policy: No electronic items: cellular telephones, Blackberrys, personal digital assistants, digital music players or similar items that may disrupt the learning environment may be used at any time for any purpose during the classroom or laboratory time. If a cell phone must be kept on due to a potential emergency situation, it must be on a silent setting. If an emergency call must be taken during a class, the student must leave the classroom prior to answering the call and not return until the call is completed. See also Article IV.B Conduct Rules and Regulations of the Student Code of Conduct at the University of Toledo.

Readings: Reading for the course is shown on the accompanying handout. Readings are to be completed prior to the lecture and lab portions of the class.

If there is a conflict or misunderstanding, see the instructor privately for a resolution.

OVERVIEW OF COURSE GRADE ASSIGNMENT

Midterm Grading

Midterm grades will be presented per university requirements and based on the current updated cumulative scores obtained by the students usually the first 5 or 6 weeks.

Final Grading

Homework 7%, Quizzes 14%, Lab 34%, Midterm Test 1 20%, Final Exam 25 % (Comprehensive)

Overall*: A >= 90, B >= 80, C > = 70, D > = 60*

Details are shown in the following table.

Assignment	Weight for each	Nbr. of assignments	Overall
Homework	1%	7	7%
Quiz	2%	7	14%
Lab reports	3.4%	10	34%
Test	20%	1	20%
Final Exam	25%	1	25%
Total:			100%

Grading for missed assignment due to an emergency: For missed assignments due to an emergency or a foreseeable event, students must fill out the missed assignments form and email the form along with written documentations from a 3rd party. **The missed assignment form must be emailed to the instructor on Monday November 23, 2019.** Final exam grade will be used in lieu of the missed assignment to calculate final grading.

Late lab reports will be accepted with a reduction of 20% per day.

Extra credit work will be given during the semester. It will be announced publicly to all the students in the same manner. There will not be extra credit for an individual or group of students. Both the midterm and final grading use the same formula, scale, and weights.

COURSE GUIDELINES

Please use your UT student email address (XX@Rockets.Utoledo.edu) for all your communications. The subject line must be***: EET2210 LastName Keyword***. E.g.: subject: EET2210 Mubenga Homework4. Homework assignments are accepted only before or on the assigned day. Homework is graded on correctness. The final answer alone is not enough to get credit. Solution steps must be shown to get credit.

When not done in person, preferred communication between the instructor and students will take place via BlackBoard and email to a student's Rocket email address. While the instructor will not communicate via email on a regular basis throughout the semester, it is advisable that students check their BlackBoard and email regularly so as to keep abreast of any special instructions, clarifications on assignments or cancellations that may occur during the term

SAFETY AND HEALTH SERVICES FOR UT STUDENTS

http://www.utoledo.edu/offices/provost/utc/docs/CampusHealthSafetyContacts.pdf

COURSE SCHEDULE

No Class Dates: September 2, October 10-11, November 11, November 27-29.
Test Date: Wednesday, October 2nd, 2019 8.00AM-9.20AM
Final Exam Date: Monday December 9, 2019 8AM-10AM

Course Schedule (Subject to Change depending on the course progress)

Date	Week	Chapter	Test	Lab	Quiz on	Homework	Assigned on	Due on
26-Aug	1	Ch.1		Lab0 : Intro. + expectations + safety+ syllabus		ch1,2	28-Aug	9-Sep
2-Sep	2	Ch.1,2		**NO LAB, NO CLASS on Mon/ Labor day**				
9-Sep	3	Ch.2,3		Lab1: Exp#2- Construction of a Logic Probe	ch1,2 Wed	ch3,4	9-Sep	23-Sep
16-Sep	4	Ch.4		Lab2: Exp#3- Number systems				
23-Sep	5	Ch.4,5		Lab3: Exp#4- Logic Gates	ch 3,4 Wed	ch5	23-Sep	30-Sep
30-Sep	6	Review 1-5	**Wed. Oct 2 8-9.20AM**	Lab 4: Exp#6-Interpreting Manufacturer's Data Sheets				
7-Oct	7	Ch.6		Lab 5: Exp#7- Boolean Laws & DeMorgan's Theorem	ch5 Mon.	ch6,7	7-Oct	21-Oct
14-Oct	8	Ch.7 BB only		Lab 6: Exp#8- Logic Circuit simplification				
21-Oct	9	Ch.7, 8		Lab 7: Exp#11- Adder and Magnitude Comparator	ch6, 7 Wed	ch8,9	21-Oct	6-Nov
28-Oct	10	Ch.8		Lab 8: Exp#12-Combinational logic using multiplexers				
4-Nov	11	Ch.9		Lab 9: Exp#14: The D latch and D flip-flop				
11-Nov	12	Ch.10:1,2,4.		**NO LAB, NO CLASS on Mon/ Vet. day**	ch8,9 Wed	ch10,11	13-Nov	20-Nov
18-Nov	13	Ch.11		Lab 10: Exp#16:The J-K flip-flop				
25-Nov	14	Ch.12		**NO LAB, NO CLASS on Wed/ Thxgiving**	ch10,11 Mon	ch12	25-Nov	2-Dec
2-Dec	15	Review 1-12			ch12 Wed			
9-Dec	16		**Mon. Dec 9 8-10AM**					

I have received and read the syllabus.

Printed Student Name……

Signature……Date……..